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歡迎蒞臨聽講

Topic:

Nanometer-Scale III-V CMOS

Speaker: Prof. J. A. del Alamo

Microsystems Technology Laboratories
Massachusetts Institute of Technology

Date: Friday, December 16th, 2016

Time: 15:00-17:00

Venue: Conference Room 201, MIRC
(電子資訊大樓 201會議室)

Abstract

In the last few years, as Si electronics faces mounting difficulties to maintain its historical scaling path, transistors based on III-V compound semiconductors have emerged as a credible alternative. To get to this point, fundamental technical problems had to be solved though there are still many challenges that need to be addressed before the first non-Si CMOS technology becomes a reality. Among them, harnessing the outstanding electron transport properties of InGaAs, the leading n-channel material candidate, towards a high-performance nanoscale MOSFET has proven difficult: contact resistance, off-state characteristics, reliability and Si integration remain serious problems. Introducing a new material system is not the only challenge, scalability to sub-10 nm gate dimensions also demands a new 3D transistor geometry. InGaAs FinFETs, Trigate MOSFETs and Nanowire MOSFETs have all been demonstrated but their performance is still disappointing. To compound the challenge, a high-performance nanoscale p-type transistor is also required. Among III-Vs, InGaSb is the most promising candidate. Planar MOSFETs have been demonstrated but more advanced geometries remain elusive. This talk will review recent progress as well as challenges confronting III-V electronics for future CMOS logic applications.

Speaker Bio

Jesús A. del Alamo is Director of the Microsystems Technology Laboratories, Donner Professor, and Professor of Electrical Engineering at Massachusetts Institute of Technology. He holds a PhD degree from Stanford University. His research interests focus on the physics, technology, modeling and reliability of new III-V and III-N field-effect transistors for future logic, communications and power switching applications. He has received the Intel Outstanding Researcher Award in Emerging Research Devices, the Semiconductor Research Corporation Technical Excellence Award and the IEEE Electron Devices Society Education Award as well as a Doctorate Honoris Causa from the Universidad Politecnica de Madrid (Spain). He is a Fellow of IEEE and APS and a member of the Royal Spanish Academy of Engineering.

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